Unit I

University Questions with Answer

Part A – 2 Marks

1. Define the following terms: Boolean variable, complement, literal

Answer:

a. Variable: The symbol which represents an arbitrary element of Boolean algebra is known as variable. Any single variable or a function of several variables can have either a 0 or 1.
   Example:
   Y = A + BC, variables A, B, and C can have either a 1 or 0 value, and function Y also can have either a 1 or 0 value.
b. Complement: A complement of a variable is represented by a "bar" over the letter. For example, the complement of variable A is represented by $\overline{A}$ or A'.
c. Literal: Each occurrence of a variable in Boolean function either in a complemented or un-complemented form is called a literal.

2. State the fundamental postulates of Boolean algebra.

Answer:

The postulates of a mathematical system form the basic assumption from which it is possible to deduce the theorems, laws and properties of the system.

a. Closure: Closure with respect to the operator + : When two binary elements are operated by operator + the result is a unique binary element.

   Closure: Closure with respect to the operator **.** (dot) : When two binary elements are operated by operator **.** (dot), the result is a unique binary element.

b. An identity element with respect to +, designated by 0: A + 0 = 0 + A = A

   An identity element with respect to **.** (dot), designated by 1: A **.** 1 = 1 **.** A = A

c. Commutative with respect to + : A + B = B + A

   Commutative with respect to **.** (dot) : A **.** B = B **.** A

d. Distributive property of **.** (dot) over + : A . (B + C) = (A **.** B) + (A **.** C)

   Distributive property of + over **.** (dot) : A + (B . C) = (A + B) **.** (A + C)

e. Associative property of + : A + (B + C) = (A + B) + C

   Associative property of **.** : A **.** (B **.** C) = (A **.** B) **.** C

f. For every binary element, there exists complement element. For example, if A is an element, we have A' is a complement of A i.e., if A = 0, then A' = 1 and vice versa.

g. There exist at least two elements, say A and B in the set of binary elements such that A not equals B.

3. State the associativity laws of Boolean algebra

Answer:

Associative property of + operator : A + (B + C) = (A + B) + C
Associative property of **.** (dot) operator: A **.** (B **.** C) = (A **.** B) **.** C

4. List down the basic theorems of Boolean algebra.

Answer:

Theorems	(a)	(b)
Theorem 1 (Idempotency)	A + A = A	A . A = 1
Theorem 2	A + 1 = A	A . 0 = 0
Theorem 3 (Involution)	(A')' = A	
Theorem 4 (Absorption)	A + AB = A	A (A + B) = A
Theorem 5	A + A'B = A + B	A . (A' + B) = AB
Theorem 6 (Associative)	A (B + C) = (A + B) + C	A (BC) = (AB) C

5. Explain De-Morgan's Theorem

Answer:

DeMorgan's Laws are used to negate compound Boolean expressions.

DeMorgan's Law:

~ (A && B) = (~A) || (~B)

~ (A||B) = (~A) && (~B)

In other words,

NOT (A AND B) = (NOT A) OR (NOT B)

NOT (A OR B) = (NOT A) AND (NOT B)

Notice that it is similar to the distributive postulate in mathematics. The not operator is distributed among both terms inside of the parentheses, except the operator switches from *and* to *or*, or vice versa.

6. Mention any two advantages of De-Morgan's Theorem

Answer:

(i) It is used in simplifying the Boolean expressions

(ii) It allows the implementation of same Boolean expression using different logic gates (NAND or NOR).

7. Define the principle of duality theorem.

Answer:

The principle of duality theorem says that, starting with a Boolean relation, another Boolean relation can be derived by using the following procedure:

a. Changing each OR sign to an AND sign

b. Changing each AND sign to an OR sign and

c. Complementing any 0 or 1 appearing in the expression.

Example: Dual of relation A + A' = 1 is A, A' = 0

8. Apply De-Morgan's theorem to simplify: $\overline{A + B\overline{C}}$

Answer:

$$\overline{A + \overline{B}C} = \overline{A} \cdot \overline{\overline{B}\overline{C}}$$

$$= \overline{A} \cdot (\overline{B} + C)$$

$$= \overline{A} \cdot \overline{B} + A\,\overline{C}$$

9. Define Boolean expression.

Answer:

Boolean expressions are constructed by connecting the Boolean constants and variables with the Boolean operations. These Boolean expressions are also known as Boolean formulas. We use Boolean expressions to describe switching function or Boolean functions.

For example, if the Boolean expression (A + B') C is used to describe thefunction f, then Boolean function is written as

f (A, B, C) = (A + B') C or f = (A + B') C

10. Write the Boolean expression for the output of the system shown in Figure below.

Answer:

C = (A + B)' . B
C = (A . B) + (B'. B)
C = A . B + 0 **Since, B. B' = 0 and A + 0 = A**
C = A . B

11. Simplify the given function: F = A'BC + A'B'C + ABC' + ABC

Answer:

F = A'BC + A'B'C + ABC' + ABC
= A'C (B + B') + AB (C' + C)
= A'C + AB

12. Simplify: x + x'y

Answer:

Z= x + x'y = x + xy + x'y since A + AB = A

Z= x + y (x + x') since x + x' = 1

Z = x + y

13. What is sum of product form?

Answer:

A product term is any group of literals that are ANDed together. For example, ABC, XY, and so on. A sum term is any group of literals that are ORed together such as A + B + C, X + Y and so on. A sum of products (SOP) is a group of product terms ORed together. For example,

f (A, B, C) = AB + AB'C'

14. What is product of sum form?

Answer:

A product of sums (POS) is any groups of sum terms ANDed together. For example,

f (A, B, C) = (A + B + C) . (B' + C)

15. What is standard SOP and POS forms:

Answer:

If each term in sum of product (SOP) form contains all the literals then the SOP form is known as standard or canonical SOP form.
If each term in Product of sum (POS) form contains all the literals then the POS form is known as standard or canonical POS form.

16. What is min term and max term?

Answer:

Each individual term in standard SOP form is called min term and each individual term in standard POS form is called max term. The concept of min terms and max terms allow us to introduce very convenient shorthand notations to express logical functions.

17. Mention the steps involved in converting SOP to standard SOP.

Answer:

Step 1: Find missing literal in each product term if any.
Step 2: AND each product term having literal (s) with term (s) form by ORing the literal and its complement
Step 3: Expand the terms by applying distributive law and reorder the literals in the product terms.
Step 4: Reduce the expression by omitting repeated product terms if any. Because A + A = A.

18. Convert the given expression in standard SOP form: f (A, B, C) = AC + AB + BC

Answer:

Step 1: Finding missing literal in each product term

AC = Literal B is missing

AB = Literal C is missing

BC = Literal A is missing

Steps 2: AND product term with (missing literal + its complement)

f (A, B, C) = AC (B + B') + AB (C + C') + BC (A + A')

Step 3: Expand the terms and reorder literals

f (A, B, C) = ABC + AB'C + ABC + ABC' + ABC + A'BC

Step 4: Omit repeated product terms (allowing only one time):

f (A, B, C) = ABC + AB'C + ABC + ABC' + ABC + A'BC Since A + A = A

f (A, B, C) = ABC + AB'C + ABC' + A'BC

19. Define: Don't care conditions.

Answer:

In some logic circuits, certain input conditions never occur; therefore the corresponding output never appears. In such cases the output level is not defined, it can be either HIGH or LOW. These output levels are indicated by 'X' or 'd' in the truth tables and are called don't care outputs or don't care conditions or incompletely specified functions.

20. Define logic gates.

Answer:

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function. The types of gates available are the NOT, AND, OR, NAND, NOR, exclusive-OR, and exclusive-NOR.

21. Write the Boolean function of an XOR gate give its truth table.

Answer:

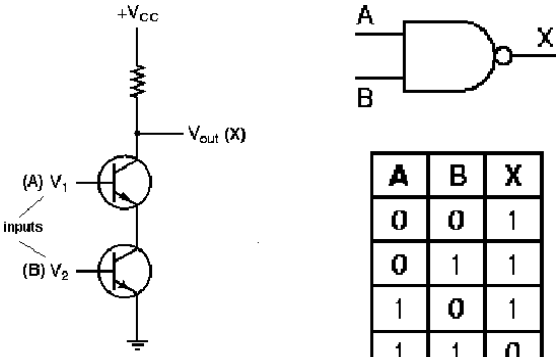
Boolean Expression: Y = AB' + A'B
Truth Table:

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

22. What are Universal gates? Give examples.

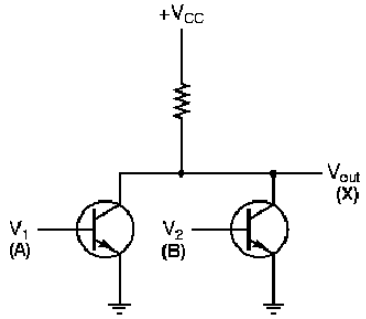
Answer:

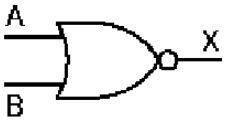
The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND and NOR gates.



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

(a) NAND Gate





A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(b) NOR Gate

23. Write the Boolean function of an NAND and NOR gate give its truth table.

Answer:

a) **NAND Gate:** Boolean Expression: Y = (A.B)'

Truth Table:

Input		Output
A	B	Y
0	0	1
0	1	1

1	0	1
1	1	0

b) **NOR Gate:** Boolean Expression: Y = (A+B)'
Truth table:

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

24. What is propagation delay of a gate?

Answer: The propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. Often this refers to the time required for the output to reach from 10% to 90% of its final output level when the input changes. Reducing gate delaysin digital circuits allows them to process data at a faster rate and improve overall performance.

25. List any two advantages of CMOS logic.

Answer:

CMOS has been and will remain the dominant technology is almost all VLSI design areas. This is a direct result of the following advantages offered by CMOS processes.

- Low power consumption: CMOS process provides lower power consumption and is easy to scaling down.
- High input impedance: Gate of MOS needs much lower driving current than base current of bipolar.
- Reduced silicon area: Scaling down increases CMOS speed and reduces the area of the chip.
- Mature technology: CMOS processes are well established and continue to become more mature. The powerful trust by leading edge digital memory and processors has led to continuous improvement and down scaling of CMOS processes.

- Design resources: Circuit and system design in CMOS is supported by a vast number of resources. Many design techniques and design libraries for analog and digital design are available.
- Availability: CMOS processes are now readily available for prototype designs through fabrication brokers, at low prices. This has boosted the design knowledge by real implementations, rather than pure theoretical treatments.
- Price: CMOS is the cheapest process available, when compared against other technologies with the same minimum feature size.

26. What does LS in 74LS00 indicate?

Answer:

IC 74LS00 is an Integrated Circuit (IC) containing four two-input NAND gates in a package. Here LS stands for Low power Schottky (LS) and 74 is the device serial number for logic gate ICs. In this family of logic gate ICs the power consumption is of the order of milli Watts (mw).

27. What is the advantage of using Schottky TTL gate?

Answer:

The junction of the transistor is prevented from heavy forward bias when it is turned ON and hence the transistor is kept out of deep / hard saturation. This has been achieved by connecting a diode across the base-to-collector junction of the transistor. Otherwise, the deep saturation would cause surplus of carriers to be stored in the base region of the transistor which causes increased propagation delay. The diode used here is the schottky diode that has very little junction capacitance and fast recovery time.

28. Write short note on tri-state gates.

Answer:

In addition to the normal output state (logic 0 and logic1), these gates can generate a third output state called High impedance (denoted by Z). These gates are having additional control input (CNTL), which when enabled produces normal output states; otherwise it makes the output into high impedance (open circuit) state. Under this condition the output becomes independent of input. The example for tri-state gate includes tri-state buffers and tri-state inverters.

Part B – 16 Marks

1. List out any four basic rules that are used in Boolean algebra expressions. (8)
2. Explain the fundamental rules used in Boolean expression (8)
3. Elaborate the basic laws of Boolean algebra with sample. (8)
4. Explain the basic laws of Boolean algebra with sample. (8)
5. Apply De-Morgan's theorem for the function $\overline{(A + B + C)}\, D$ (3)
6. Write the steps for simplifying a logic expression using Karnaugh map. (10)
7. Find the minimum sum of products expression using K-map for the function F=∑m(7,9,10,11,12,13,14,15) and realize the minimized function using only NAND gates.
8. Obtain simplified POS using k-map for
   F (a, b, c, d) = ∑ (0, 2, 3, 4, 8, 10, 12, 13, 14)
9. Find the reduced SOP form of the following function: f(A, B, C, D) = ∑m(1, 3, 7, 11, 15) + ∑d(0, 2, 4).
10. Simplify using Quine-McClusky method F = ∑m(0, 1, 2,3,10, 11,12,13,14,15) (16)
11. Simplify using tabulation method. F (V, W, X, Y, Z) = ∑(4, 5, 6, 7, 9, 10, 14, 19, 26, 30, 31) **Note:** Quine-McClusky method is also called tabulation method (16)
12. Realize XOR function using four NAND gates only. (4)
13. Simplify the following functions and draw the logic diagram for the same. (6)
    F1 = f(A, B, C) = ∑ (1, 2, 3, 5)
    F2 = f(A, B, C) = ∑ (1, 3, 5, 7)
    F3 = f(A, B, C) = ∑ (2, 3, 4, 5)

14. Explain the precautionary measures to be considered while handling CMOS device (5)
15. Draw the circuit diagrams of 2-input CMOS NOR gate and CMOS NAND gate using CMOS logic and explain their operation. (8)
16. What are the different types of TTL gates available? Explain their operation using suitable example. (8)
17. Explain the working of TTL Tristate gate. (12)
18. Compare the performance characteristics of TTL and CMOS (8)
19. List out and explain the data sheet parameters. (11)
20. Implement the expression (8)
    (i) AB + BCD + EFGH
    (ii) (A + B) (C + D +E) (F + G + H + I)
    with gates.
21. Explain the procedure for converting binary to gray code number and gray code to binary number with sample.

Some Additional Two mark Questions:

2. Determine the decimal value of the fractional number 0.1011

Answer: 1 0 1 1

$1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4}$

$= 1 \times (0.5) + 0 \times (0.25) + 1 \times (0.125) + 1 \times (0.0625)$

$= 0.5 + 0.125 + 0.0625$

$= (0.6875)_{10}$

3. Convert 1000_2 into Gray code and Excess 3 code

Answer:

(i) Gray Code conversion:

1 0 0 0 = 1 (1 xor 0) (0 xor 0) (0 xor 0)

= (1 1 0 0)

- **Note:** The *most significant bit* (left-most bit) in the gray code is the same as the corresponding digit in binary.
  - Going from left to right, XOR each adjacent pair of binary digits to get the next Gray code digit.

(ii) Excess 3 code conversion:

Add three (011_2) with the given Binary number

1000 011 = (1011) – Excess 3 code.

4. Convert the Gray coded number 10011011 to its binary equivalent.

Answer:

The rules of conversion from Gray code to binary are given in the Gray code summary

- The Gray code number has 8 bits so the Binary equivalent will also have 8 bits
- The *most significant bit* (left-most bit) is the same in both cases

- The next-to-most significant bit in the binary number comes from adding the most significant bit in the binary number to the next-to-most significant bit in the Gray coded number, the sum is noted and any carry ignored.
- Generally, working from *left to right* i.e. from most significant bit to least significant bit, then the nth bit (counting from right to left) in the binary number is formed from summing the n+1th bit in the binary number with the nth bit in the Gray coded number. The corresponding sum is noted and any carry ignored.

In the case of this example,

Gray Code 10011011 Binary Digit 1 = 1 (same as Gray code)
Gray Code 10011011 Binary Digit 2 = 0 + 1 = 1
Gray Code 10011011 Binary Digit 3 = 0 + 1 = 1
Gray Code 10011011 Binary Digit 4 = 1 + 1 = 0 (carry 1)
Gray Code 10011011 Binary Digit 5 = 1 + 0 = 1
Gray Code 10011011 Binary Digit 6 = 0 + 1 = 1
Gray Code 10011011 Binary Digit 7 = 1 + 1 = 0 (carry 1)
Gray Code 10011011 Binary Digit 8 = 1 + 0 = 1

and hence

$10011011_{gray} = 11101101_{bin}$

5. Convert $(367)_{10}$ into Excess 3 code.

Answer:

The given decimal number is to be converted to BCD first. Then it can be converted into excess 3 code.

$(367)_{10}$ = 0011 0110 0111 – Excess 3 code

Adding 3 to the Lower nibble makes it excess 3 code.

```
0011 0110 0111
          0011  (+)
--------------
```

0011 0110 1010 = The last digit is not a valid BCD code. Hence add 6 in the last digit.

0011 0110 1010

0110 (+)

---

^{11} 1 0000 = $(370)_{10}$

6. Which gate is equal to AND-invert Gate?

Answer:

NAND gate.

7. Which gate is equal to OR-invert Gate?

Answer:

NOR gate.

8. Bubbled OR gate is equal to----------

Answer:

NAND gate

9. Bubbled AND gate is equal to----------

Answer:

NOR gate

10. Mention the important characteristics of digital IC's?

Answer:

(i) Fan out
(ii) Power dissipation
(iii) Propagation Delay
(iv) Noise Margin
(v) Fan In
(vi) Operating temperature
(vii) Power supply requirements

11. Define Fan-out?

Answer:

Fan out specifies the number of standard loads that the output of the gate can drive without impairment of its normal operation.

12. Define power dissipation.

Answer:

Power dissipation is a measure of power consumed by the gate when fully driven by all its inputs.

13. What is propagation delay?

Answer:

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

14. Define noise margin?

Answer:

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

15. Define fan in?

Answer:

Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

16. What is Operating temperature?

Answer:

All the gates or semiconductor devices are temperature sensitive in nature. The temperature in which the performance of the IC is effective is called as operating temperature. Operating temperature of the IC vary from 0^0 C to 70^0 c.

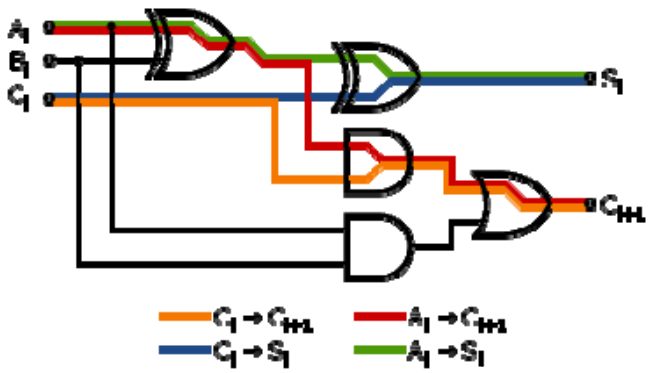
17. What is High threshold logic?

Answer:

Some digital circuits operate in environments, which produce very high noise signals. For operation in such surroundings there is available a type of DTL gate which possesses a high threshold to noise immunity. This type of gate is called HTL logic or High Threshold Logic.

18. Some additional Information on Propagation delay:

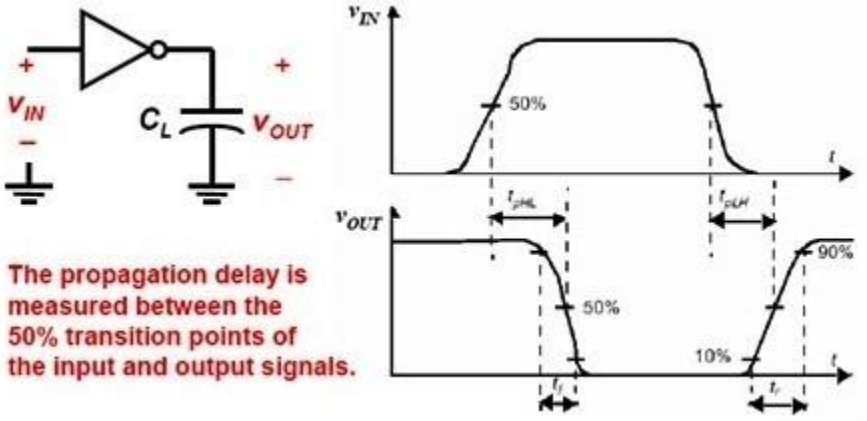
The difference in *propagation delays* of logic elements is the major contributorto glitches in asynchronous circuits as a result of race conditions.



A full adder has an overall gate delay of 3 logic gates from the inputs *A* and *B* to the carry output C_{out} shown in red.

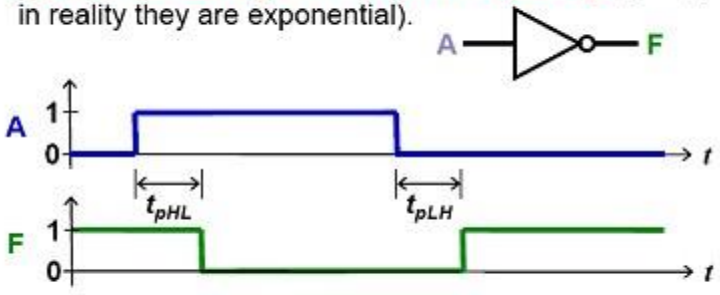
Propagation delay:

When an input signal of a logic gate is changed, there is a propagation delay before the output of the logic gate changes. This is due to capacitive loading at the output.



Propagation Delay in Timing Diagrams

- To simplify the drawing of timing diagrams, we can approximate the signal transitions to be abrupt (though in reality they are exponential).



To further simplify timing analysis, we can define the propagation delay as $t_p = (t_{pHL} + t_{pLH})/2$

Product	CMOS technology generation	Clock frequency, *f*	Fan-out=4 inverter delay
Pentium II	0.25 μm	600 MHz	~100 ps
Pentium III	0.18 μm	1.8 GHz	~40 ps
Pentium IV	0.13 μm	3.2 GHz	~20 ps

Table 1: Examples of Propagation Delay

Part A: Additional Two Mark Questions for students practice

1. Minimize the function using Boolean algebra f = x (y + w'z) + wxz
2. Find the complement of A + BC + AB
3. Convert the gray code number 11011 to binary.
4. Determine the decimal value of the fractional binary number 0.1011.
5. A certain gate draws 2mA when its output is high and 3.6mA when its output is low. What is the average power dissipation if V_{cc} is 5 V and it is operated on a 50 % duty cycle?
6. Implement 2 input XOR gate using NAND-NAND logic.
7. State Shannon's expansion theorem.
8. Expand the given Boolean function using Shannon's expansion theorem.
   F (A, B, C, D) = AB' + (AC + B) D
9. Realize OR gate using NAND gates only.

Unit II

University Questions with Answer

Part A

1. What are the major categories of digital circuits?

Answer:

The digital circuits basically of two types namely

(i) Combinational circuits

(ii) Sequential circuits

2. What is combinational circuit?

Answer:

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage or feedback involved, the resulting circuit is called combinational circuit.

A combinational circuit consists of input variables, logic gates, and output variables. The logic gates accept signals from the input variables and generate output signals.

3. Differentiate combinational and sequential circuits.

Answer:

S. No	Combinational circuits	Sequential circuits
1	In combinational circuits, the output variables are at all times dependent on the combination of input variables	In sequential circuits, the output variables depend not only on the present input variables but they also depend upon the past history of input variables
2	Memory unit is not required in combinational circuits	Memory unit is required to store the past history of input variables in sequential circuits
3	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits

4	Combinational circuits are easy to design	Sequential circuits are comparatively harder to design
5	Parallel adder is combinational circuit	Serial adder is a sequential circuit

4. Narrate the combinational circuit design procedure.

Answer:

Step 1: problem definition
Step 2: The determination of number of available input variables and required output variables.
Step 3: Assigning letter symbols to input and output variables
Step 4: The derivation of truth table indicating the relationships between input and output variables.
Step 5: Obtain simplified Boolean expression for each output.
Step 6: Obtain the logic diagram.

5. Design a half adder.

Answer:

The Half-adder takes two single bit inputs, let us name it as A and B. It generates two single bit outputs that are sum and carry respectively.

Truth table:

Input		Output	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Obtaining Boolean expression for each output variable

Carry = A . B
Sum = A' . B + A. B'

Using AND gate for carry output and XOR gate for sum output, we can realize the Boolean expressions and hence we get the desired logic circuit.

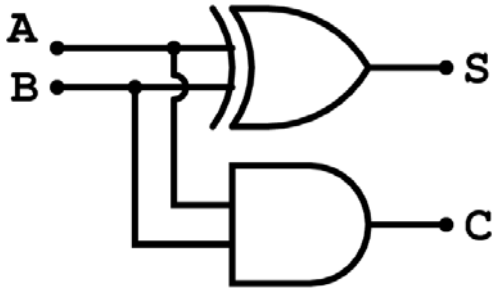


Figure: Half Adder Logic Diagram

6. What is the limitation of half adder?

Answer:

In multi-digit addition we have to add two bits along with the carry of theprevious digit addition. Effectively such addition requires addition of three bits. This is not possible with half-adder. Hence half-adders are seldom used in practice.

7. Write an expression for borrow and difference in a full subtractor circuit.

Answer:

Difference = A XOR B XOR $Borrow_{in}$

$Borrow_{out}$ = (A XNOR B) . $Borrow_{in}$

8. What is parallel Adder?

Answer:

A single full-adder is capable of adding two one-bit numbers and an input carry. In order to add binary numbers with more than one bit, additional full-adders must be employed. A n-bit parallel can be constructed using number of full adder circuits connected in parallel.

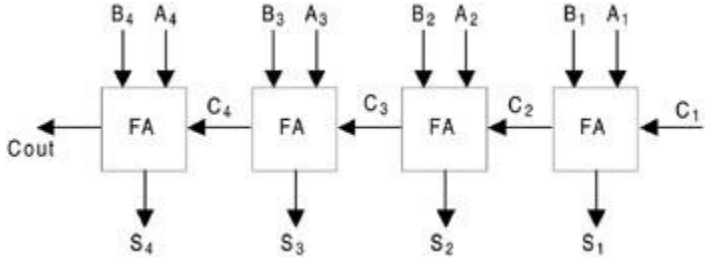


Figure: Four bit Parallel Adder

9. What is the drawback in binary parallel adder? How it can be rectified?

Answer:

The parallel adder is ripple carry adder in which the carry output of each full- adder stage is connected to the carry input of the next higher-order stage. Therefore, the sum and carry outputs of any stage cannot be produced until the input carry occurs; this leads to time delay in the addition process. The delay is known as carry propagationdelay.

One method of speeding up the process by eliminating inter stage carry delay is called look-ahead carry addition. This method utilizes logic gates to look at the lower order bits of the augend and addend to see if a higher-order carry is to be generated.

10. Compare binary serial adder and parallel adder.

Answer:

S. No	Serial Adder	Parallel Adder
1	Serial adder uses shift registers	Parallel adder uses registers with parallel load
2	The serial adder requires only one full-adder circuit	The number of full adder circuits in the parallel adder equal to the number of bits in the binary numbers
3	The serial adder is a sequential circuit	Excluding the registers, the parallel adder is a purely combinational circuit
4	Time required for addition depends on number of bits	Time required for addition does not depend on number of bits.
5	It is slower	It is faster

11. Write short note on 1-bit multiplier.

Answer:

1-Bit multiplier truth table:

A	B	Y
0	0	0

0	1	0
1	0	0
1	1	1

From the above table, the Boolean expression of multiplier output y is derived as,

Y = A.B

This can be implemented using a 2-input AND gate.

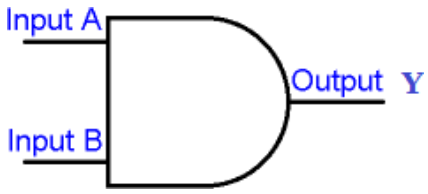


Figure : 1-Bit Multiplier (AND Gate)

12. What is a data selector?

Answer:

Multiplexer is a digital switch. Particularly, it has 2n input lines and n selection lines whose bit combinations determine which input line is selected and routed onto available only single output line.

Hence multiplexer is a selector of one out of several data sources available at its input lines, to connect it to output line. Simply it is a many to one device and also called 'data selector'.

13. Design a 2 input NAND gate using 2:1 multiplexer.

Answer:

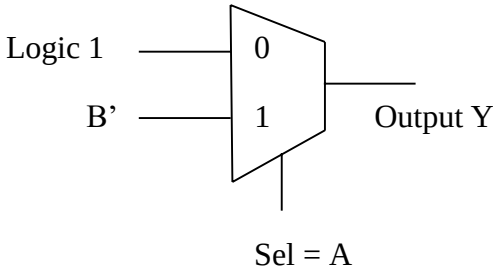
Truth table of NAND gate:

Input		Output
A	B	Y
0	0	1

0	1	1
1	0	1
1	1	0

From the above table, we can say that in a NAND gate when the input A is at logic 0, the output becomes logic 1. When the input A is at logic 1 then the output is the complement of the input B.

Therefore if we take A as select input of a 2-to-1 multiplexer, at first data input (when select input is 0) we connect logic 1 (V_{dd} supply), in the second data input (when select input is 1) we connect B in its complemented form (B'). Hence the multiplexer act as 2-input NAND gate.



14. Give an application each for a multiplexer and a demultiplexer.

Answer:

The multiplexer can also be used in the construction of any Boolean function is SOP form. Multiplexers are used as a data selector. Multiplexers are also used in time-division multiplexing at the transmitting end. They are used in A/D and D/A converters.

The demultiplexer is used as a data distributor. It is also used in time-division multiplexing at the receiving end. Demultiplexers can be used as a decoder. It can also be used to implement Boolean expressions.

15. List some of the commonly used multiplexer ICs.

Answer:

IC Number	Function
74150	16:1 multiplexer
74151	8:1 Multiplexer

74153	Dual 4:1 multiplexer
74157	Quad 2-input multiplexer

16. What is demultiplexer?

Answer:

A demultiplexer is a circuit that receives information on a single line and transmits this information to one of 2^n possible output lines. The selection of specific outputline is controlled by the values of n selection lines.

17. What is decoder?

Answer:

A decoder is a multiple-input, multiple output logic circuit which converts coded inputs into coded outputs, where the input and output codes are different. In a binary decoder n-inputs produce 2^n (or fewer) output lines. Usually, a decoder is provided with enable inputs to activate decoded output.

18. What will be the maximum number of outputs for a decoder with a 6-bit data word?

Answer:

$2^6 = 64$

19. What do you mean by encoder?

Answer:

An encoder is a digital circuit that performs the inverse operation of a decoder. Encoder has 2^n (or fewer) input lines and n output lines. Encoder has enable inputs to activate encoded outputs.

20. What is a priority encoder?

Answer:

A priority encoder is an encoder circuit in which if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

21. Distinguish between a demultiplexer and decoder.

Answer:

S. No	Decoder	Demultiplexer
1	Decoder is a many inputs to many outputs device	Demultiplexer is a one input to many output device
2	There are no selection lines	The selection of specific output line is controlled by the value of selection line

22. What are the applications of decoders?

Answer:

a. Code converters

b. Implementation of combinational circuits

c. Address decoding

d. BCD to 7-segment decoder

23. List the types of decoder ICs.

Answer:

IC number	Function
74138	3:8 decoder
74139	Dual 2:4 decoder
7442	BCD to decimal decoder
7447	BCD to 7-segment decoder

24. What are parity generators and parity checkers?

Answer:

A circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker. It must be

noted here that a parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1s either odd or even.

25. What is the need for code converters?

Answer:

There is a wide variety of binary codes used in digital systems. Some of these codes are binary-coded decimal (BCD), excess-3, Gray code and so on. Many times itis required to convert one code to another.

26. What do you mean by comparator?

Answer:

It is a special combinational circuit designed primarily to compare the relative magnitudes of two binary numbers. An n-bit comparator receives two n-bit binary A and B, and the outputs are: A > B, A < B, and A = B. As per the magnitudes of the two numbers, one of the three outputs will be high.

PART – B (16 – Marks)

1.	Design a full adder	(7)
2.	Implement the full adder using two half adders	(8)
3.	Design a full subtractor circuit and draw necessary truth tables.	(7)
4.	Draw and explain the working of carry look ahead adder	(10)
5.	Draw and explain serial adder and subtractor	(8)
6.	Design an 8-bit BCD adder using 4-bit binary adder	(8)
7.	Design a multiplier circuit to multiply the following binary number A = A0A1A2 and B = B0B1B2B3 using required number of binary parallel adders.	(10)
8.	Perform 1100 / 11 using restoring algorithm	(8)
9.	Using non-restoring division algorithm, compute 23/5.	(8)

10.	Give the comparison between restoring and non-restoring division	(4)
11.	Explain 4:1 multiplexer with the help of logic circuit and truth table	(8)
12.	Implement the function with a multiplexer. F (A, B, C, D) = ∑(0, 1, 3, 4, 8, 9, 15)	(6)
13.	Draw the diagram and explain 1 to 16 Demultiplexer circuit	(8)
14.	Explain 1:8 demultiplexer using two 1:4 demultiplexers	(4)
15.	Implement full adder using demultiplexer	(6)
16.	Draw the 3 to 8 decoder and explain	(8)
17.	Implement Boolean function F = ∑ m (1, 2, 3, 7) using 3:8 decoder	(4)
18.	Explain even parity checker.	(6)
19.	Design a binary to BCD converter	(8)
20.	Design a logic circuit to convert the 8421 BCD to excess-3 code.	(12)
21.	Design and implement a 8421 to Gray code converter. Realize the converter using only NAND gates.	(16)
22.	Design a logic circuit to convert BCD to Gray code	(16)
23.	Design a 1-bit comparator using basic gates.	(4)
24.	Explain the operation of a 4-Bit magnitude comparator circuit	(6)

Some Additional Two mark Questions

1. Define multiplexer and multiplexing.

Answer:

Multiplexing is defined as the process of feeding several independent signals to a common load, one at a time. The device or switching circuitry used to select and connectone of these several signals to the load at any one time is known as a multiplexer.

2. What is BCD adder?

Answer:

BCD (Binary Coded Decimal) Adder is a digital combinational circuit that is used for the addition of two numbers in binary coded decimal arithmetic's. BCD is a class of binary encodings of decimal numbers where each decimal digit is shown by a fixed number of bits, usually four or eight, although other sizes such as six bits have been used

Two marks Questions for students practice

1. Show that the dual of Ex-OR gate is equivalent to its complement.
2. What is tri-state logic?
3. Design a parity generator for transmitting a three bit input data.
4. Design a 4 x 1 multiplexer for the Boolean function $F = \sum (0, 2, 3, 5, 7)$
5. Convert the function F = A + BC into SOP form (standard).
6. Convert the function F = A + BC into POS form (standard).
7. Draw the logic diagram of a half subtractor circuit.
8. Write down the truth table of a 4-to-2 encoder.
9. How Carry look-ahead adder is faster than ripple carry adder?

Unit III

University Questions with Answer

Part A

1. **What is the need for sequential circuits?**

   Answer:

   There are many applications in which digital outputs are required to be generated in accordance with the sequence in which the inputs signals are received. This requirement cannot be satisfied using a combinational logic system. Theseapplications require outputs to be generated that are not only dependent on the present input conditions abut also depend upon the past history of these inputs. The past history is provided by feedback from the output back to the input.

2. **Give any two examples of sequential circuits.**

   Answer:

   The counters and registers are the common examples of sequential circuits.

3. **Define clock.**

   Answer:

   A clock is a particular type of signal that oscillates between a high and low state. It is utilized to coordinate actions of circuits. It is produced by a clock generator circuit. The most common clock signal is in the form of a square wave with a 50% dutycycle, usually with a fixed, constant frequency.

4. **Define clock period.**

   Answer:

   The time required to complete one cycle is called ‘clock period’ or clock cycle. Ideally the clock signal should have sharp transitions from one level to other.

5. **What is flip-flop?**

   Answer:

   The memory element used in sequential circuits is a flip-flop which is capable of storing 1-bit binary information.

6. Write short note on basic bi-stable element

Answer:

The basic bi-stable element has two outputs Q and Q'. It has two cross-coupled inverters, i.e., the output of the first inverter is connected as an input to the second inverter and the output of the second inverter is connected as an input to the first inverter. The basic bi-stable element is used in latches and flip-flops.

7. What is gated SR latch?

Answer:

In the conventional SR latch output changes occur immediately after the input changes occur i.e., the latch is sensitive to its S and R inputs at all times. However, in many applications it is necessary to modify the SR latch such that it is sensitive to its inputs (S and R) only when an enable input is active. Such a latch with enable input isknown as gated SR latch.

8. What is the operation of D flip-flop?

Answer:

In d flip-flop during the occurrence of clock pulse if D = 1, the output Q is set and if D = 0, the output is reset.

9. Compare latches and flip-flops.

Answer:

S. No	Latch	Flip-flop
1	A simple latch is the basis for flip-flop building	Flip-flop is built by connecting some additional components around a latch
2	Latch is level triggered either positive level or negative level triggered	Flip-flop is pulse or clock edge triggered either positive edge or negative edge triggered
3	The latch output responds to inputs, until active level is maintained at the enable input	Flip-flop output responds to inputs only at the specified (positive or negative) edges of clock pulse

10. What is the operation of JK flip-flop?

Answer:

When J input is low and K input is low the output does not change.

When J input is low and K input is high the Q output of flip-flop is reset.

When J input is high and K input is low the Q output of flip-flop is set.

When both J and K inputs are high, the output toggles on the next positive clock edge.

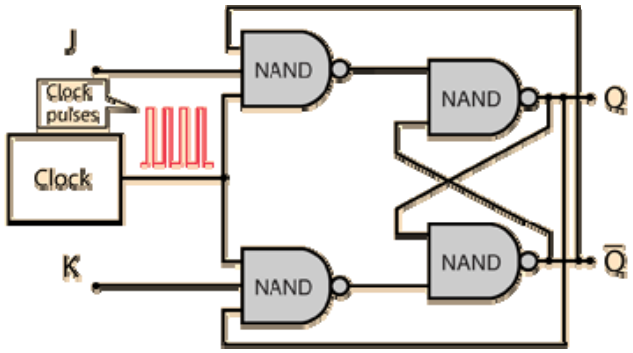
11. How does a JK Flip-flop differ from an SR flip-flop in its basic operation?

Answer:

The uncertainty in the state of an SR flip-flop when S = R = 1 is eliminated, by introducing toggle state for the same inputs (i.e., when J = K = 1) in the case of JK flip-flop.

12. Draw the logic circuit of a clocked JK flip-flop.

Answer:



13. What is race-around condition?

Answer:

In a level triggered JK flip-flop, when J and K are both high, then the output toggles continuously. This condition is called a race around condition.

14. What is a master-slave flip-flop?

Answer:

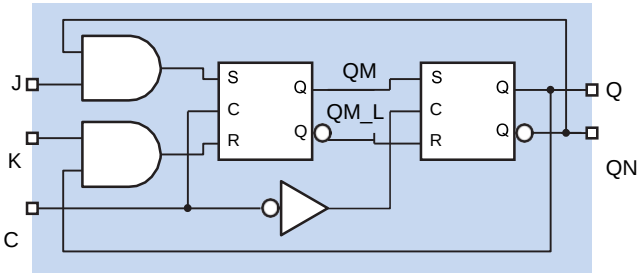
A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave. The output of the master flip-flop is fed as an input to the

slave flip-flop. The master flip-flop is triggered at the positive edge of the clock and slave flip-flop is triggered at the negative edge of the clock.

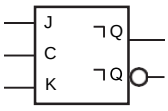
15. Draw the logic diagram of a master slave JK flip-flop.

Answer:

(a) (b) (c)



J	K	C	Q	QN
x	x	0	last Q	last QN
0	0	⊓	last Q	last QN
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	last QN	last Q



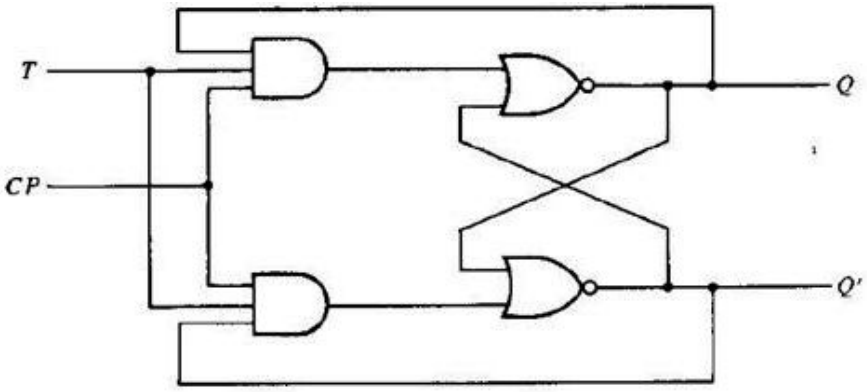
16. Write short note on asynchronous or direct inputs.

Answer:

When power is turn ON, the state of the flip-flop is uncertain. It may come to set (Q = 1) or reset (Q = 0) state. In many applications, it is necessary to initially set or reset the flip-flop. Such initial state of flip-flop can be accomplished by using the direct or asynchronous inputs of the flip-flop. These inputs are preset and clear. They can be applied at any time between clock pulses and are not in synchronism with the clock.

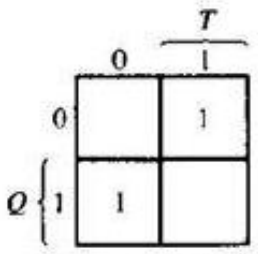
17. Draw the T-flip flop using NAND gates. Also write its characteristics equation.

Answer:



Q	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

(b) Characteristic table



$Q(t+1) = TQ' + T'Q$

(c) Characteristic equation

Characteristics Equation: Q (t+1) = T Q'(t) + T' Q(t)

18. Write the characteristic equation of SR, D, JK and T flip-flop.

Answer:

SR flip-flop: Q (t+1) = S + R' Q(t)
D flip-flop: Q (t+1) = D
JK flip-flop: Q (t+1) = J Q'(t) + K' Q(t)
T flip-flop: Q (t+1) = T Q'(t) + T' Q(t)

19. Draw the application / excitation table of SR flip-flop

Answer:

Qn	**Qn+1**	**S**	**R**
0	**0**	**0**	**X**
0	**1**	**1**	**0**
1	**0**	**0**	**1**
1	**1**	**X**	**0**

20. Obtain the excitation table of D flip-flop.

Answer:

Qn	**Qn+1**	**D**
0	0	0
0	1	1
1	0	0
1	1	1

21. Draw the excitation table of T flip-flop.

Answer:

Qn	**Qn+1**	**T**
0	0	0
0	1	1
1	0	1
1	1	0

22. Give the meaning for edge triggering in flip-flops.

Answer:

In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock pulse at the clock input. There are two types of edge triggering, namely, Positive edge triggering and negative edge triggering.

23. Convert a T-FF into an S-R FF. Draw the circuit.

Answer:

S	R	Present state Q	Next state	T flip-flop inputs
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	X	X
1	1	1	X	X

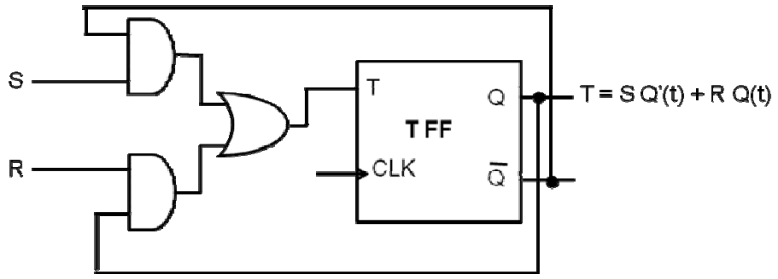
Using 3 – variable K-map to derive the Boolean expression for T – input of the flip-flop.

K-map simplification:

SR	00	01	11	10
Q = 0	0	1	x 3	1 2
Q = 1	4	1 5	x 7	6

T = S.Q'(t) + R.Q(t)

Logic Diagram:



24. Write the characteristic equation of JK Flip-flop and show how JK FF can be converted into T-FF.

Answer:

Characteristics Equation of JK FF: Q (t+1) = J Q'(t) + K' Q(t)

T	Present state	Next state	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

Deriving Boolean expression for each input of the JK flip-flop:

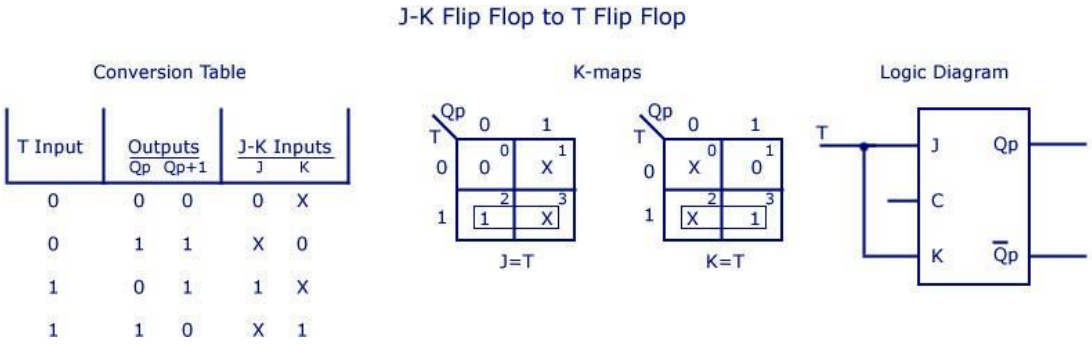
0	X
1	X

J = T

X	0
X	1

K = T

Therefore by connecting the J and K inputs of the JK flip-flop directly we can obtain T – Flip flop.



25. If the input frequency of a T FF is 1600 kHz, what will be the output frequency? Give reason for your answer.

Answer:

800 kHz. As the T- FF toggles at every clock pulse, it acts as a clock divider.

26. Define register.

Answer:

A group of flip-flops connected together forms a register. A register is used solely for storing and shifting data which is in the form of 1's and/or 0's, entered from an external source. It has no specific sequence of states except in certain very specialized applications.
A flip-flop can store 1-bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information / number containing n-bits.

27. Define counter.

Answer:

A counter is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. On arrival of each clock pulse, the counter is incremented by one. In case of sown counter it is decremented by one.

28. Define asynchronous counter.

Answer:

A binary asynchronous / ripple counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the clock input of next higher-order flip-flop. The flip-flop holding the least significant bit receives the incoming clock pulses.

29. Define synchronous counter.

Answer:

When counter is clocked such that each flip-flop is triggered at the same, the counter is called as synchronous counter. Here clock signal is connected in parallel to clock inputs of all the flip-flops.

30. Differentiate synchronous and asynchronous counters.

Answer:

S. No	Asynchronous counter	Synchronous counter
1	In this type of counter flip-flops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of next flip-flop.
2	All the flip-flops are not clocked simultaneously.	All the flip-flops are clocked simultaneously.
3	Logic circuit is very simple even for more number of states.	Design involves complex logic circuit as number of states increases.
4	Main drawback of these counters is their low speed as the clock is propagated through the number of flip-flops before it reaches last flip-flop.	As clock is simultaneously given to allflip-flops there is no problem of propagation delay. Hence they are highspeed counters and are preferred when number of flip-flops increases in the givendesign.

31. Define modulus of a counter.

Answer:

The total number of counts or stable states a counter can indicate is called 'Modulus'. The term 'modulo' is used to describe the count capability of counters. For example, mod-6 counter goes through states 0 to 5 and mod-4 counter goes through states 0 – 3.

32. What is the minimum number of flip-flops needed to design a counter of modulus 60?

Answer:

$2^n >= 60$
Therefore n = 6.

33. What is meant by programmable counter? Mention its application.

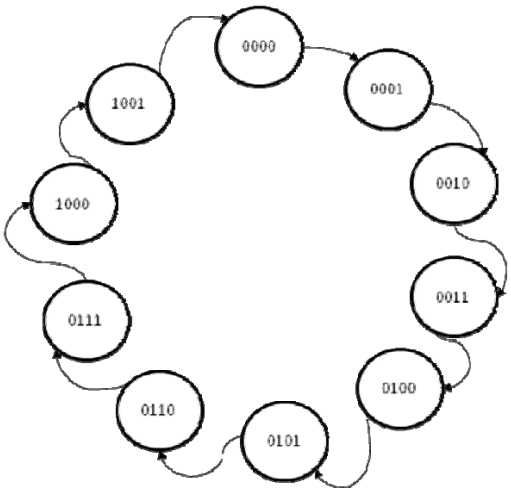
Answer:

A counter that divides an input frequency by a number which can be programmed is called programmable counter.
Applications of programmable counter:

1. Frequency division
2. Digital clock
3. Stop watch
4. Programmable logic controllers

34. Draw the state diagram of a Mod-10 counter.

Answer:



35. The propagation delay of each flip-flop is 50 ns, determine the maximum operating frequency for mod-32 ripple counter.

Answer:
We know that mod-32 uses five flip-flops. With propagation delay (t_{pd}) = 50 ns, the maximum operating frequency (f_{max}) for ripple counter can be given as,

$$F_{max}\ (_{ripple}) = 1 / 5 \times 50 \text{ ns} = 4 \text{ MHz}.$$

36. Defined controlled buffer register.

Answer:

We can control input and output of a register by connecting tri-state devices at the input and output sides of the register. This register is called controlled buffer register.

37. Define shift register.

Answer:

The binary information (data) in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of movement or shifting is essential for certain arithmetic and logical operations used in microprocessors. This gives rise to a group of registers called shift registers.

38. What are the different types of shift registers? (or) Classify the registers with respect to serial and parallel input output.

Answer:

There are five types,

(i) Serial in serial out

(ii) Serial in parallel out

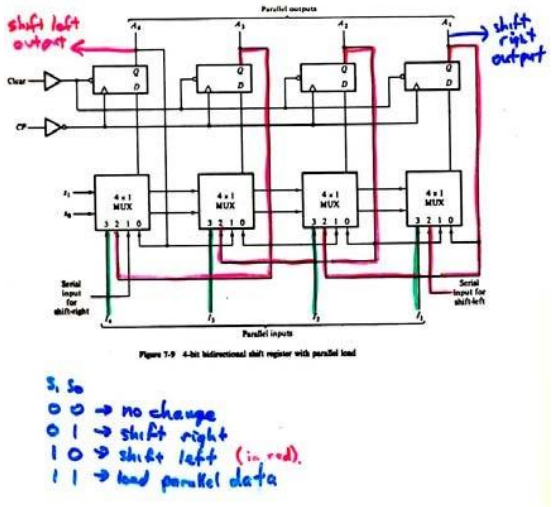
(iii) Parallel in serial out

(iv) Parallel in parallel out

(v) Bidirectional shift register

39. Draw the logic diagram of 4 – bit universal shift register.

Answer:



40. Mention the applications of shift registers.

Answer:

(i) Delay line

(ii) Serial to parallel converter

(iii) Parallel to serial converter

(iv) Pseudo random binary sequence generator

(v) Sequence detector

41. What is shift register counter?

Answer:

A shift register can also be used as a counter. A shift register with the serial output connected back to the serial input is called shift register counter. The most common shift register counters are the ring counter and the Johnson counter.

PART – B (16 – Marks)

1.	Explain the operation of a 1-bit memory cell.	(8)
2.	Draw the logic diagram of Gated SR latch using NAND gates and explain.	(6)
3.	Draw the clocked RS flip-flop and explain its operation	(10)
4.	Derive the characteristic equation of a SR flip-flop.	(8)
5.	Draw the logic diagram of a D – FF using NAND gates and explain.	(6)
6.	Explain the working of JK flip-flop.	(8)
7.	Draw the logic diagram for a master slave flip-flop and explain.	(8)
8.	Write short note on level and edge triggering.	(4)
9.	Convert a D-FF into JK flip-flop.	(8)
10.	Convert a D-FF into T flip-flop.	(6)
11.	Explain in detail the operation of a 4-bit binary ripple counter.	(16)
12.	Explain in detail the operation of a 3-bit binary synchronous counter.	(16)

13. Design a BCD up/down counter using SR flip-flops. (16)

14. Design an asynchronous mod-12 counter. (8)

15. Design BCD ripple counter using JK flip-flop. (16)

16. Design a mod – 10 synchronous counter and draw the timing diagram of it. (16)

17. Design a 3-bit synchronous up / down counter using T –FF (10)

18. Explain the types of shift registers. (6)

19. Draw a 4-bit serial-in serial-out shift register and explain. (8)

20. Draw a 4-bit parallel-in serial-out shift register and briefly explain. (8)

21. Draw the logic diagram for a 5-bit serial load shift right register using D flip-flop and explain. (8)

22. Draw the 8-bit serial in – parallel out shift register and explain its operation. (8)

23. Draw the logic diagram of a 4-bit parallel load re-circulating shift register and explain. (8)

24. Explain the operation of Universal shift register with neat block diagram. (10)

25. Design a six stage ring counter and explain its operation. Mention about the use of presetting the counter. (16)

26. Draw the four bit Johnson or twisted ring counter and explain the operation. (8)

27. Design a 3-bit binary counter using T flip-flop that has a repeated sequence of six states. 000 – 001 – 010 – 100 – 101 – 110. Give the state table, state diagram and logic diagram. (16)

28. Design a synchronous counter which counts in the sequence 0, 2, 6, 1, 7, 5, 0 ….. using D-FFs. Draw the logic diagram and state diagram. (8)

29. Design a synchronous counter using JK flip-flop to count the following sequence 7, 4, 3, 1, 6, 0, 7 ….. (8)

Part A: Additional Two Mark Questions for students practice

1. Convert a JK flip-flop to D flip-flop
2. Draw the timing diagram for a mod-4 asynchronous up counter.

Unit IV

University Questions with Answer

Part A - Two marks

1. **Write short note on memory.**

   Answer:

   Memories are made up of registers. Each register in the memory is one storage location also called memory location. Each memory location is identified by an address. Generally, the number of bits that a memory can store is its capacity. Most ofthe times the capacity is specified in terms of bytes (group of eight bits).

2. **Define a memory cell. Give an example.**

   Answer:

   Each register consists of storage elements (flip-flops or capacitors in semiconductor memories and magnetic domain in magnetic storage), each of which stores one bit of data. A storage element is called a cell.

3. **How the semiconductor memories are classified?**

   Answer:

Semiconductor memories			
Non-volatile memory		Volatile memory	
Read only memory (ROM)	Read / Write Memory (NVRAM)	Read / Write memory (RAM)	
Mask programmable ROM	EPROM	Random Access	Non-random access
Programmable ROM	EEPROM	SRAM	FIFO
	Flash	DRAM	LIFO
			Shift Register

4. **Whether ROM is classified as a non-volatile storage device? Why?**

   Answer:

   Yes. The ROM is is Non-volatile storage device (memory), since it can hold data even if power is turned off.

5. Mention the two types of erasable PROM.

Answer:

(i) UV – Erasable PROM (EPROM or UVPROM)

(ii) Electrically Erasable PROM (EEPROM)

6. Define EEPROM.

Answer:

Electrically Erasable programmable ROMs also use MOS circuitry very similar to that of PROM. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level than erasing all the information since the information can be changed by using electrical signals.

7. Distinguish between EPROM and EEPROM.

Answer:

Both EPROM and EEPROM are programmed in the same way (electrically). However, the erasing mechanism is different in these two memories. In the case of EPROMs the erase is done via Ultra Violet (UV) light source, where as EEPROMs can be programmed and erased electrically using field emission.

Many EPROM Chips are encapsulated in plastic that is opaque to UV light and are one time programmable.

8. What is RAM? (or) What is Random access memory?

Answer:

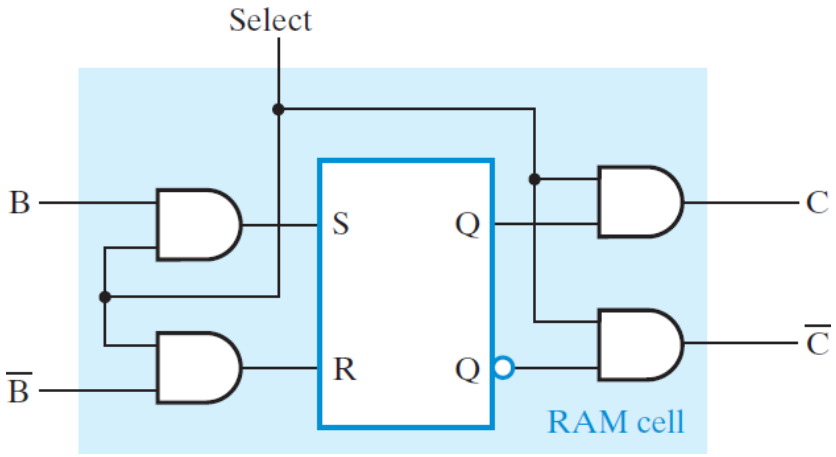
The volatile memories which can hold data as long as power is ON are called RAMs. These memories allow both read and write operation many time. There are two types of RAMs:

Static RAM

Dynamic RAM

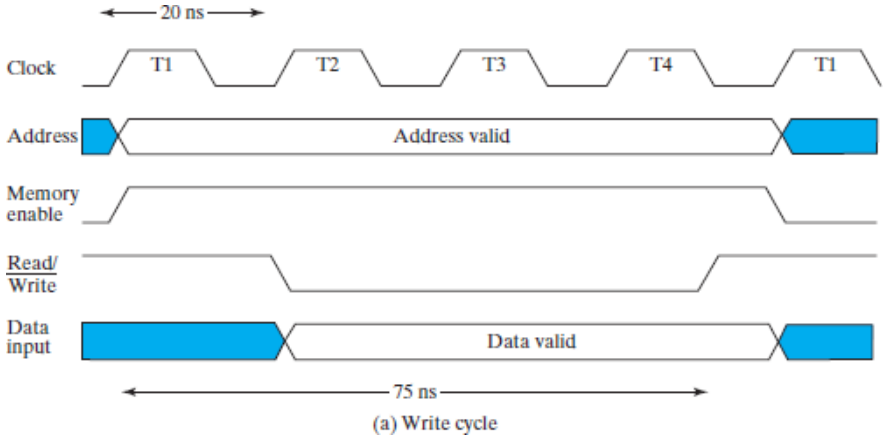
9. Draw the structure of typical RAM cell.

Answer:



10. Explain 'write operation' with an example.

Answer:



(a) Write cycle

11. What is access time and cycle time of a memory?

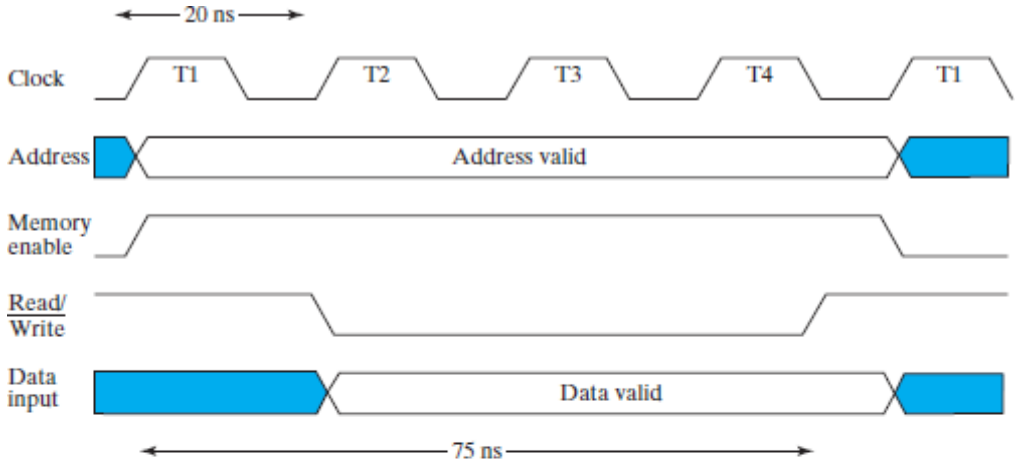
Answer:

Access time:
Memory access time is corresponding to the time interval between the read/write request and the availability of the data.

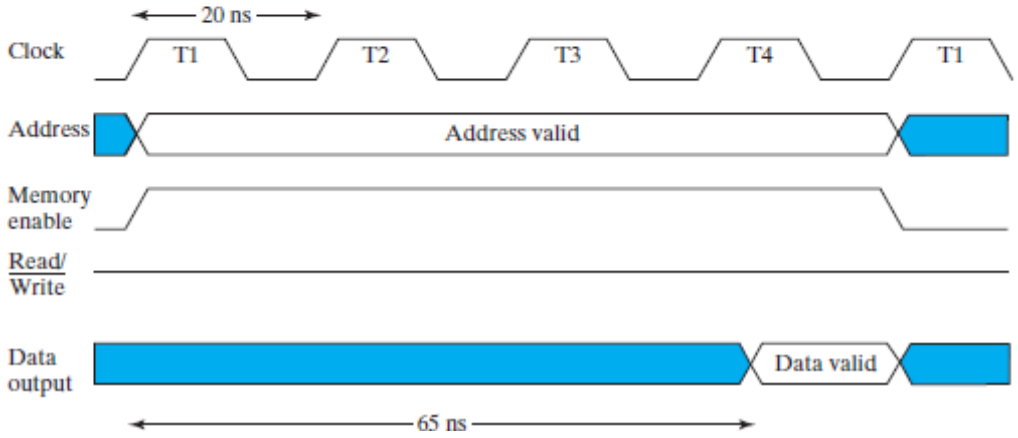
Cycle time:
Cycle time is the time, usually measured in nanoseconds, between the start of one random access memory (RAM) access to the time when the next access can be started

12. Draw the timing waveforms of read and write operation of a memory.

Answer:



(a) Write cycle



(b) Read cycle

13. What is the size of the decoder in a 32 x 10 ROM?

Answer:

5: 32 Decoder

14. How many locations are addressed using 18 address lines?

Answer:

The number of locations addressed = 2^{18} = 262144.

15. What is meant by memory expansion? Mention its limit.

Answer:

It is possible to expand size of memory by connecting two or more ICs together. The memory expansion can be achieved in two ways: By expanding word size and by expanding memory capacity.
(i) Expanding Word Size:
The word size of memory IC can be increased by connecting two memory ICs such a way that their data bus is in series and address bus in parallel.
(ii) Expanding memory capacity:
The memory capacity can be increased by connecting two or more memory ICs in parallel i.e., by connecting address, data and control lines in parallel to all memory ICs.

The memory devices are interfaced with processors and are accessed using address, data and control bus provided by the processor. Each processor has defined number of address lines and data lines. Suppose a processor has 24 address lines and 16 data lines, we can expand memory word size up to 16 and we can expand memorycapacity up to 2^{24} = 16 bytes.

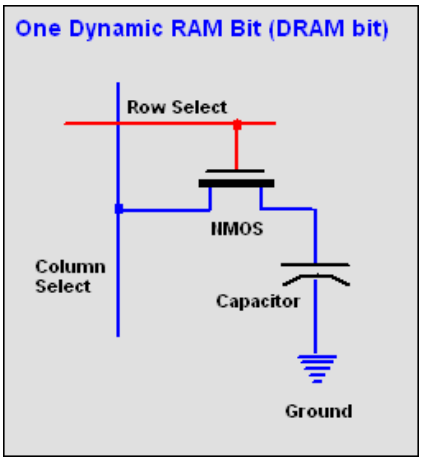
16. Calculate the number of address lines and data lines for 2 G byte memory.

Answer:

Address lines = 31
Data lines = 8

17. Draw the block diagram of Dynamic RAM cell.

Answer:



18. Explain static memory.

Answer:

Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.

19. Compare and contrast static and dynamic memory. (or) What is the difference between static RAM and Dynamic RAM?

Answer:

S. No	Static RAM	Dynamic RAM
1	Static RAM contains less memory cells per unit area	Dynamic RAM contains more memory cells per unit area as compared to Static RAM
2	It has less access time hence faster memories	Its access time is greater than static RAMs
3	Static RAM consists of number of flip-flops. Each flip-flop stores one bit	Dynamic RAM stores the data as a charge on the capacitor. It consists of MOSFET and a capacitor for each cell
4	Refreshing circuitry is not required	Refreshing circuitry is required to maintain charge on the capacitors after every milliseconds.
5	Cost is more	Cost is less

20. Compare fixed function ICs, ASIC and PLD approaches.

Answer:

Comparison parameter	Fixed function IC approach	ASIC Approach	PLD approach
Development cost	Low	High	Low
Space required	Large	Minimum	Less
Power required	Large	Less	Less
Reliability	Less compared to other two approaches	Highest	High
Circuit testing	Easy	Specialized testing methods are required whichmay increase cost and effort	Easy
Design flexibility	Less	No	More
Design time	Less	More	Less

21. What are the types of PLDs?

Answer:

According to architecture, complexity and flexibility in programming PLDs are classified as
(i) PROMs
(ii) PLAs
(iii)PALs
(iv)FPGAs
(v) CPLDs

22. What is PAL? How does it differ from PLA? (or) What is the difference between PAL and PLA? (or) Compare the structure of PAL and PLA.

Answer:

Programmable array logic (PAL) is a programmable device with a fixed OR array and a programmable OR array. Because only AND gates are programmable, the PAL is easier to program, but is not as flexible as the PLA. On the other hand, PLA is a programmable device with a programmable AND array and programmable OR array.

23. Differentiate between PROM, PAL and PLA

Answer:

Sl. No	PROM	PAL	PLA
1	AND array is fixed and OR array is programmable	OR array is fixed and Only AND arrays is programmable	Both AND as well as OR arrays are programmable
2	Cheaper and simple to use	Cheaper and simpler	Costliest and complex than PAL and PROMs
3	All minterns are decoded	AND arrays can be programmed to get desired minterms	AND arrays can be programmed to get desired minterms
4	Only Boolean functions in standard SOP form can be implemented using PROM	Any Boolean functions in SOP form can be implemented using PAL	Any Boolean functions in SOP form can be implemented using PLA

24. State the importance of FPGA.

Answer:

The FPGAs allow the user to program the chip in the field i.e., place where the chip is going to be used. Compared to standard gate arrays, the field programmable gate arrays are larger devices. They are more flexible and can be used for more complex implementations of logic circuits that use equivalent of several Lakhs of logic gates.

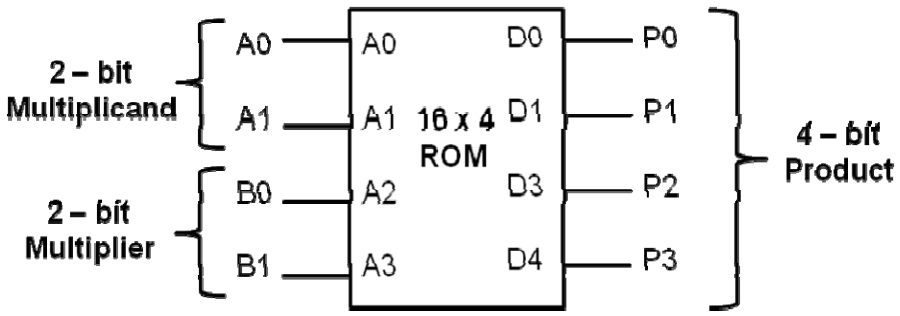
25. Implement a 2-bit multiplier using ROM.

Answer:

The 2-bit multiplier truth table is shown below:

A1	A0	B1	B0	Y3	Y2	Y1	Y0
0	0	X	X	0	0	0	0
X	X	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

As shown in the table, the 2-bit multiplier takes two 2-bit numbers as input and generates a four bit output. Therefore this circuit needs a 4 –input address and 16 memory locations to store the possible results and 4 – output lines as a product result. In other words, 16 possible outputs, each with 4-bit size.



26. Implement the exclusive-OR function using ROM.

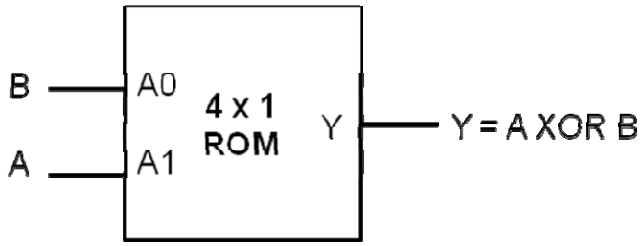
Answer:

Here the XOR generates 4 possible outputs and each output is of size 1-bit.

Hence the required ROM structure is as shown below.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Truth table of XOR gate



PART – B (16 – Marks)

1. Write short note on semiconductor memories. (6)
2. Categorize RAM and ROM and explain in detail. (8)
3. Illustrate the concept of 16 x 8 bit ROM arrange with diagram. (8)
4. Describe the typical ROM internal organization with necessary diagram. (8)
5. Briefly explain EPROM and EEPROM technology. (6)
6. Elaborate the single fused PROM cell with clear sketch. (6)
7. Write a note on RAM. (8)
8. Describe the RAM organization. (10)
9. Explain the basic structure of 256 x 4 static RAM with neat sketch. (16)
10. Explain read and write operation of memory with timing waveforms. (8)
11. Describe the two dimensional address decoding scheme of typical DRAM in detail. (8)

12. Explain:

    (i) Memory decoding (6)

    (ii) Explain the various ROM organizations and give the uses for each type. (10)

13. We can expand the word size of a RAM by combining two or more RAM chips. For instance, we can use two 32 x 8 memory chips where the number 32 represents the number of words and 8 represents the number of bits per word, to obtain a 32 x 16. In thiscase the number of words remain the same but the length of each word will two bytes long. Draw a block diagram to show we can use two 16 x 4 memory chips to obtain a 16x 8 RAM. (8)

14. Explain the principle of operation of a bipolar SRAM cell. (8)

15. Explain the principle of operation of a MOSFET SRAM cell. (8)

16. Explain in detail about PLA and PAL. (8)

17. Write short notes on PAL. (8)

18. Write a note on FPGA. (8)

19. Briefly explain about FPGA with a neat block diagram. (16)

20. Explain the following terms:

    a) Dynamic memory

    b) Volatile storage

    c) Field programmable

    d) Mask programmable

21. Design a combinational circuit using a ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. (16)

22. Design a full adder using a suitable PROM. (8)

23. Implement the given functions using PROM (16)

    $F1 = \sum (0, 1, 3, 4, 6, 7)$

    $F2 = \sum (1, 2, 3, 5)$

24. Implement the following Boolean functions with a PLA. (16)

F1 (A, B, C) = $\sum$ (0, 1, 2, 4)

F2 (A, B, C) = $\sum$ (0, 5, 6, 7)

F3 (A, B, C) = $\sum$ (0, 3, 5, 7)

25. Implement the following functions using three inputs, four product terms and two output PLA. (8)

F1 = AB' + AC + A'BC'

F2 = (AC + BC)'

26. A combinational circuit is defined by functions (16)

F1 (A, B, C) = $\sum$ (3, 5, 6, 7)

F2 (A, B, C) = $\sum$ (0, 2, 4, 7)

Implement the circuit with a PLA having three inputs, four product terms and two outputs.

PART A – Additional Two mark Questions

1. **Compare EPROM, EEPROM and Flash memory**

Answer:

EPROM = Erasable Programmable Read-Only Memory (erasable by exposure to ultraviolet light)

EEPROM = Electrically EPROM (erasable by using the proper electrical signals)

Flash = memory that is static in nature (after taking power away it retains the values), but can be easily changed just like the dynamic memory in everyday computers without additional wires.

2. **Why PAL was developed?**

Answer:

PAL is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

3. **What is FPGA?**

   Answer:

   FPGA stands for field programmable gate array, which is the very recent family of devices, added in the programmable logic devices. The word field refers to the ability of the gate arrays to be programmed for a specific function by the end user. The word array indicates a series of columns and rows of gates that can be programmed by the end user.

4. **List the configurable elements in the FPGA architecture.**

   Answer:

   FPGA architecture consists of three types of configurable elements:

   1. Programmable Input / Output blocks (IOBs)
   2. Programmable configurable logic blocks (CLBs)
   3. Programmable interconnections

5. **How is individual location in a EEPROM programmed or erased?**

   Answer:

   Since it is electrically erasable memory, by activating particular row and column it is possible that individual location can be programmed or erased.

6. **What is registered PAL?**
   Answer:

   Some PALs have flip-flops at the output. The flip-flops store the output. The several flip-flops at the output form a register and because these outputs have tri- state buffers, the output of register can be controlled. Such PALs are referred to as registered PALs.

Part A: Additional Two Mark Questions for students practice

1. Distinguish between static RAM and dynamic RAM.
2. Write the advantages of EPROM over a PROM. What is need for address multiplexing?
3. What is mask programmable?
4. What are the advantages of static RAM compared to Dynamic RAM? A bipolar RAM chip is arranged as 16 words. How many bits are stored in the chip?
5. Why the input variables to a PAL are buffered?

PART B Additional 16 Mark Questions

1. Briefly explain about various types of ROM and RAM cells. (16)
2. Given the 32 x 8 ROM chip with enable input, show the external connection necessary to construct a 128 x 8 ROM with four chips and a decoder. (8)
3. Construct a 5 x 32 decoder with four 3 x 5 decoders and a 2 x 4 decoder. Use block diagrams. (10)
4. With logic diagram, explain the basic Macro cell. (6)
5. Write a short note on SRAM based FPGA (8)
6. Draw the logic diagram of Xilinx 4000 CLB and I/O blocks and explain their function. (16)
7. Details briefly about field programmable gate arrays. (16)
8. Draw the PLA circuit to implement the functions (16)

   F1 = A'B + AC' + A'BC'

   F2 = (AC + AB + BC)'
9. A combinational circuit is defined as the functions (16)

   F1 = AB'C' + AB'C + ABC

   F2 = A'BC + AB'C + ABC

   Implement the digital circuit with a PLA having three inputs, three product terms and two outputs.
10. Obtain the PLA programming table for the combinational circuit with following functions

    A (x, y, z) = $\sum$ (1, 2, 4, 6) (8)

    B (x, y, z) = $\sum$ (0, 1, 6, 7)

    C (x, y, z) = $\sum$ (2, 6)

    D (x, y, z) = $\sum$ (1, 2, 3, 5, 7)
11. Obtain the PLA program table with only seven product terms for a BCD to excess-3 code converter. Also give the fuse map. (16)